IN THE CLAIMS:

1. (Previously Presented) A method of reducing recess relief within an interconnect structure located in a layer of a semiconductor device, comprising:

planarizing a layer of conductive material located within an opening and over an upper surface of a dielectric layer, said planarizing forming an interconnect structure and leaving residue over said upper surface;

removing at least a portion of said residue from said upper surface using a post planarization clean, said removing forming a recessed interconnect structure and thereby forming a recessed substrate; and

conducting a recess reduction etch to remove a portion of said recessed substrate to reduce a relief of said recessed substrate.

2. (Original)The method as recited in Claim 1 wherein said recess reduction etch forms a substantially planar surface about said interconnect structure.

3. (Previously Presented)The method as recited in Claim 2 further including forming a metal-insulator-metal capacitor over said interconnect structure, subsequent to said conducting said recess reduction.

4. (Original)The method as recited in Claim 1 wherein said recess reduction etch includes using a gas mixture comprising a gas compound containing fluorine, argon and nitrogen

or hydrogen.

5. (Previously Presented)The method as recited in Claim 4 wherein said recess reduction etch is a plasma etch and a flow rate of said gas compound containing fluorine is about 20 sccm, said argon is about 100 sccm and said nitrogen or said hydrogen is about 100 sccm.

6. (Original)The method as recited in Claim 4 wherein said gas compound is a fluorinated hydrocarbon compound.

7. (Original)The method as recited in Claim 6 wherein said fluorinated hydrocarbon compound is CH_2F_2.

8. (Original)The method as recited in Claim 1 wherein said recess reduction etch is conducted for about 10 seconds.

9. (Original)The method as recited in Claim 1 wherein said removing is conducted under substantially non-oxidizing conditions.

10. (Original)The method as recited in Claim 1 wherein a depth of said recess subsequent to said recess reduction etch ranges from about 3 nm to about zero nm.

11. (Withdrawn) A capacitor, comprising

a first conductive layer located on an interconnect structure formed in a dielectric layer, wherein a surface of said dielectric layer is substantially planar about said interconnect structure located in a dielectric layer;

a capacitor dielectric layer located over said first metal layer; and

a second conductive layer located over said capacitor dielectric layer.

12. (Withdrawn)The capacitor as recited in Claim 11 wherein a depth of a recess within a perimeter of said interconnect structure ranges from about 3.0 nm to about zero nm.

13. (Withdrawn)The capacitor as recited in Claim 11 a thickness of said first conductive layer ranges from about 20 nm to 100 nm.

14. (Withdrawn)The capacitor as recited in Claim 11 wherein said interconnect structure is a contact plug.

15. (Withdrawn)The capacitor as recited in Claim 14 wherein said contact plug comprises tungsten having a barrier layer between said tungsten and said dielectric layer .

16. (Previously Presented)A method of fabricating an integrated circuit, comprising:

forming transistors on a semiconductor substrate;

depositing a dielectric layer over said transistors;

forming a layer of conductive material within an opening in said dielectric layer and over an upper surface of said dielectric layer;

planarizing said layer of conductive material, said planarizing forming an interconnect structure and leaving residue over said upper surface;

removing at least a portion of said residue from said upper surface using a post planarization clean, said removing forming a recessed interconnect structure and thereby forming a recessed substrate;

conducting a recess reduction etch to remove a portion of said recessed substrate to reduce a relief of said recessed substrate; then

forming a metal-insulator-metal capacitor on at least a portion of said interconnect structure.

17. (Original)The method as recited in Claim 16 wherein said recess reduction etch includes using a gas mixture comprising a fluorinated hydrocarbon, argon and nitrogen or hydrogen.

18. (Original)The method as recited in Claim 17 wherein said recess reduction etch is a plasma etch and a flow rate of said fluorinated hydrocarbon is about 20 sccm, said argon is about 100 sccm and said nitrogen or said hydrogen is about 100 sccm.

19. (Original)The method as recited in Claim 17 wherein said recess reduction etch is conducted under substantially non-oxidizing conditions.

20. (Original)The method as recited in Claim 16 wherein a depth of said recess subsequent to said recess reduction etch ranges from about 3 nm to about zero nm.